FIG. 1

FIG. 2

34 — RAM core

14

32 — Clock buffer

From CPU

36 — Processor (MPU)

From CPU

38 — I/O

To bus

FIG. 3

Use of memory in a single memory space

| A | g1 | B | C | g3 | D | g4 | E | g5 | F | g6 | G |

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

g2

Total memory size:	32 words
Used memory:	20 words
Unused memory:	12 words
Available memory:	3 words

FIG. 4

Use of memory in a single memory space

Space ID

001 A
002 B
003 C
004 D
005 E
006 F
007 G

Total memory size:	32 words
Used memory:	20 words
Unused memory:	12 words
Available memory:	12 words

FIG. 5

← Inserted element

FIG. 6

+(modify value: increment by 1(one)) ⇒

Virtual array

FIG. 7

FIG. 8A

Processor (MPU) 36

Space ID control table

Physical memory cell

Memory module 14

34

FIG. 8B

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags
010	100	60	0	164	R
010	160	4	80	164	R
016	0	20	60	20	RW
...	...	...	...	...	...
212	0	100	360	100	RW
-	-	-	-	-	-
-	-	-	-	-	-

Access control flag legend:
R: Read only
W: Write only
RW: Read/Write enabled

FIG. 8C

Content of physical memory cell

Physical address	ID	Logical address		
0	010:0100	10		Space ID 010
1	010:0101	21		
	...	...		
59	010:0159	33		
60	016:0000	2323		Space ID 016
	...	...		
79	016:0019	3241		
80	010:0159	15		Space ID 010
	...	...		
83	010:0163	8		
	...	...		
360	212:0000	-589		Space ID 212
459	212:0099	-1022		
	...	...		

FIG. 9A

CPU 12

Space ID + address

Memory module group
14-n
14-2
14-1

FIG. 9B

36

Space ID + address

Space ID comparator 52

Address comparator 54

Address calculator 56

34

On-chip storage cell

FIG. 9C

CPU 12

Data

Memory chip group
14-n
14-2
14-1

10/088028

FIG. 10C

Virtual array

Space ID = 010

20	010:0000
21	010:0001
...	
33	010:0059
38	010:0060
15	010:0061
...	
62	010:0149

FIG. 10A

Space ID 010

100	...	
101	20	010:0000
	21	010:0001
	...	
159	33	010:0059

Logical Allocated On-chip
Space ID start   region   physical start Total size
          address size   address

...	...	...	...	...
010	0	60	100	150
...	...	...	...	...

Memory module 14—i

FIG. 10B

Space ID 010

10	...	
11	38	010:0060
	15	010:0061
	...	
99	62	010:0149

Logical Allocated On-chip
Space ID start   region   physical start Total size
          address size   address

...	...	...	...	...
010	60	90	10	150
...	...	...	...	...

Memory module 14—j

FIG. 11

Start

1101 — Accept/interpret instruction

1102 — Look up space ID

1103 — Pertains to self?

No → End

Yes

1104 — Necessary checks

1105 — Error present?

Yes → 1106 — Error report → End

No

1107 — Compare range to be deleted with range of elements stored in own RAM

1108 — Comparison results

A → NOP (1109) → End

B → Update allocated region size (1110) → End

C → Decrease logical start address (1111) → End

D → Update logical start address, physical start address (1112)

E → Update allocated region size (1113) → End

F → F

FIG. 12A

Range occupied by elements in own chip

Range subject to deletion

FIG. 12B

1201

1202

Range occupied by elements in own chip

Range subject to deletion

FIG. 12E

Range subject to deletion

Range occupied by elements in own chip

FIG. 12C

Range subject to deletion

Range occupied by elements in own chip

FIG. 12F

Range occupied by elements in own chip

Range subject to deletion

FIG. 12D

Range subject to deletion

Range occupied by elements in own chip

FIG. 13

E

F

1114

Delete data in space ID control table

1115

Update data in space ID control table

End

FIG. 14

```
                    ╭─────────╮
                    │  Start  │
                    ╰─────────╯
                         │
1401 ─────┐   ┌──────────────────────────┐
          └─→ │ Accept/interpret instruction │
              └──────────────────────────┘
                         │           1402
              ┌──────────────────────────┐
              │     Look up space ID      │
              └──────────────────────────┘
                         │
                    ◇───────────◇   1403
            No     ╱ Pertains to self? ╲
        ┌──────────◇───────────◇
        │                │ Yes
        ↓                │
   ╭─────────╮           │
   │   End   │    1404   │
   ╰─────────╯   ┌──────────────────────────┐
                 │     Necessary checks      │
                 └──────────────────────────┘
                         │
1405 ─────┐         ◇───────────◇          1406
          └──────→ ╱ Error present? ╲  Yes
                    ◇───────────◇────────┐
                         │ No            │
1407 ─────┐             │    ┌──────────────────────┐
          │             │    │    Error report       │
          │        ◇───────────◇    └──────────────────────┘
          │       ╱ Add to own RAM? ╲            │
    No    └───────◇───────────◇                  │
    ┌────────────────│ Yes                       ↓
    │         ┌──────────────────────┐      ╭─────────╮
    │         │   Update space ID     │      │   End   │
    │         │    control table      │      ╰─────────╯
    │         └──────────────────────┘
    │              │        1408
    │         ┌──────────────────────┐
    │         │    Store data in      │
    │         │     RAM core          │
    │         └──────────────────────┘
    │              │        1409
    └──────────────┤
      1410    ┌──────────────────────┐
              │  Update "Total size"  │
              └──────────────────────┘
                         │
                    ╭─────────╮
                    │   End   │
                    ╰─────────╯
```

FIG. 15A

FIG. 15B

FIG. 16A

PMM-1(14-1)

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags	Region of physical memory
010	0	20	10	n*10	R	10 Atlanta
-	-	-	-	-	-	20 Austin

PMM-X(14-X)

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags	Region of physical memory
010	(n-2)*10	20	50	n*10	R	50 Chicago
-	-	-	-	-	-	60 Cincinnati

1501

ID=10
0 Atlanta
1 Austin
...
n-2 Chicago
n-1 Cincinnati

FIG. 16B

PMM-1(14-1)

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags	Region of physical memory
011	0	20	30	m*10	R	30 Helena
-	-	-	-	-	-	40 Houston

PMM-X(14-X)

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags	Region of physical memory
011	(m-2)*10	20	30	m*10	R	30 Washington
-	-	-	-	-	-	40 Wichita

1510

ID=11
0 Helena
1 Houston
...
m-2 Washington
m-1 Wichita

FIG. 17

FIG. 18

PMM-1(14-1)

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags	Region of physical memory
010	0	20	10	n*10	R	10 Atlanta
-	-	-	-	-	-	20 Austin

...

PMM-X(14-X)

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags	Region of physical memory
010	(n-2)*10	20	50	n*10	R	50 Chicago
-	-	-	-	-	-	60 Cincinnati

ID=10

0	Atlanta
1	Austin
...	
n-2	Chicago
n-1	Cincinnati

Division point

FIG. 19

PMM-1(14-X)

1911

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags	Region of physical memory
010	0	20	10	(n-1)*10	R	10 Atlanta
-	-	-	-	-	-	20 Austin

PMM-X(14-X)

1912

Space ID	Logical start address	Allocated region size	On-chip physical start address	Total size	Access control flags	Region of physical memory
010	(n-2)*10	10	50	(n-1)*10	R	50 Chicago
011	0	10	60	10	R	60 Cincinnati
-	-	-	-	-	-	

1913

...

1901

ID=10
0 Atlanta
1 Austin
...
n-2 Chicago

1902

ID=11
0 Cincinnati

FIG. 20

FIG. 21

FIG. 22

Virtual array 2

Virtual array 1

Physical array	Converted flag

Subscript conversion

1
5
...
...
123

1
0
: :
: :
0

Value modification

Subscript conversion

1
0
: :
: :
0

Value modification

...

FIG. 23

FIG. 24

First bus   Second bus   Third bus   2304

First memory module group   Second memory module group   Third memory module group   Fourth memory module group

Record No. array

0	8
1	5
...	...
n-1	123

Record No. →

Array of pointers to value list

	Record No.	Pointer to value list
0	3	
1	26	
...	...	...
m-1	4	

Record No. →

Count array

	Record No.	Storage location
0	N(0)	
1	N(1)	
...	...	
m-1	N(m-1)	

Sorted record No. array   2410

0	S(0)
1	S(1)
...	...
n-1	S(n-1)

FIG. 25

| Record No. array | Array of pointers to value array | Value list (occupation) |

FIG. 27

2701

First bus

2702

IN OUT

First memory module group   Second memory module group

Search conditions: surname starting with H to K

	Value list			Yes/No flag array
0	Franklin		0	0
1	Hill		1	1
...	...		...	...
...	...		...	...
n-1	Smith		m-1	0

FIG. 26

Bus 1

Bus 2

IN OUT IN OUT IN OUT

IN OUT IN OUT IN OUT

IN OUT

2601

2602

2603

First memory module group

Second memory module group

Third memory module group

Record No. array

0	8
1	5
...	...
...	...
n-1	123

Record No.

Array of pointers to value list

0	3	
1	26	
...	...	
...	...	
m-1	4	

Record No.
Space ID

ID=10000

0	S(0)
1	S(1)
...	...
...	...

ID=10001

0	S(0)
1	S(1)
...	...
...	...

ID=9999+m

0	S(0)
1	S(1)
...	...
...	...

FIG. 28

First bus

Second bus   2704

Third bus   2702

2705

2703

Third memory module group

Fourth memory module group

Second memory module group

Fifth memory module group

Record No.
array

0	8
1	5
⋮	⋮
⋮	⋮
n-1	123

Record No.

Array of pointers
to value list

	Record No.
	Pointer to value list
0	3
1	26
⋮	⋮
⋮	⋮
m-1	4

Record No.

Yes/No flag array

	Record No.
	(Only for a match)
0	0
1	1
⋮	⋮
⋮	⋮
m-1	0

Record No.

Hit information storage array

0	1
1	0
⋮	⋮
⋮	⋮
n-1	1